

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	23326	(716/1-7; 714/25-57; 324/755,765; 702/108-126).ccls.	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/10/20 11:14
L2	1409	(hdl or vhdl or verilog or (hardware adj description adj language)) same (RTL or (register adj transfer adj level))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/10/20 11:17
L3	344909	(fault or error or redundan\$5) same (detect\$4 or check\$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/10/20 11:19
L4	481	2 and 3	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/10/20 11:20
L5	229	4 and 1	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/10/20 11:21
L6	59	5 and FPGA	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/10/20 11:21
L7	6	(add\$3 or insert\$3 or adapt\$3) same (fault\$3 or error\$3 or redundan\$5) same circuit and 6	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/10/20 11:23



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Thu, 20 Oct 2005, 4:09:19 PM EST

Search Query Display

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		Results
<u>#1</u>	(fault tolerant RTL VHDL HDL<IN>metadata)	0
<u>#2</u>	((fault tolerant<in>metadata) <and> (rtl<in>metadata))<and> (vhdl<in>metadata)	1
<u>#3</u>	((fault tolerant<in>metadata) <and> (rtl<in>metadata))<and> (vhdl<in>metadata)	1

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